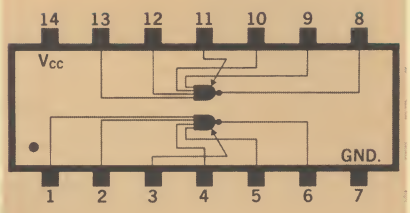
LOW POWER MONOLITHIC DTL ELEMENT

DUAL EXPANDABLE FOUR-INPUT NAND GATE

NE416A

OCTOBER 1966

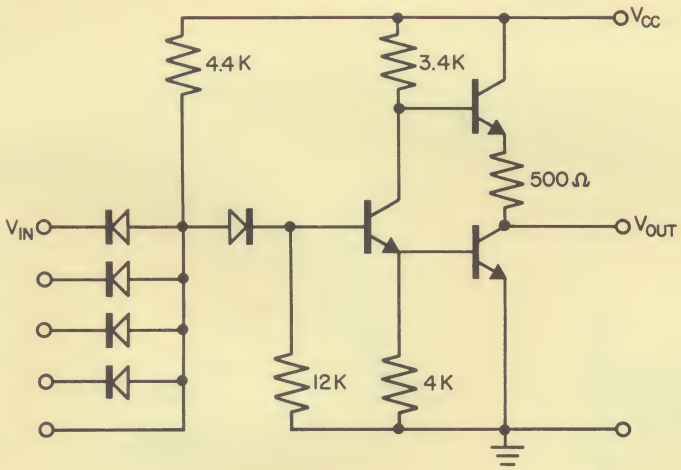


The NE416A is a monolithic semiconductor integrated circuit designed for use in low power digital systems. The element provides for input expansion capability in the NE400A logic system. Input expansion elements from the NE100A logic family may be used for expansion of the NE416A.

The same planar and epitaxial techniques used in fabricating the SE400J-Series elements are employed in making the NE400A-Series. These elements are tested under the appropriate portion of Signetics established SURE Program (Systematic Uniformity and Reliability Evaluation), as described in Bulletin No. 5001. Acceptance Test Sub-Groups called out in the tabular data refer to selection and test criteria as specified in Table II of SURE Program Bulletin No. 5001.

BASIC CIRCUIT SCHEMATIC

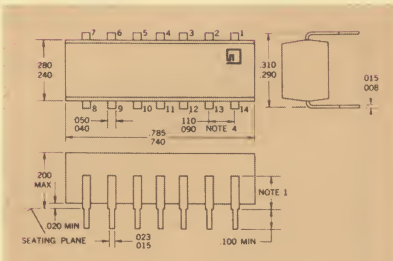
NOTE: ½ of NE416A shown. Component values are typical.



ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE	6.0V	OPERATING TEMP.	0°C to +70°C
V_{cc}	6.0V	STORAGE TEMP.	-65°C to +150°C
INPUT CURRENT	±10mA	θ JUNCTION TO CASE	0.2°C/mW
OUTPUT CURRENT	+30, -10mA	JUNCTION TEMP.	150°C

Maximum ratings are limiting values above which serviceability may be impaired.



NOTE:
1. Lead spacing shall be measured within this zone.
2. Molded Plastic Body.
3. Kovar Leads.
4. Lead spacing tolerances are non-cumulative.
5. Thermal resistance from junction to still air, Θ_{J-A}= 0.16°C/mW

NE416A

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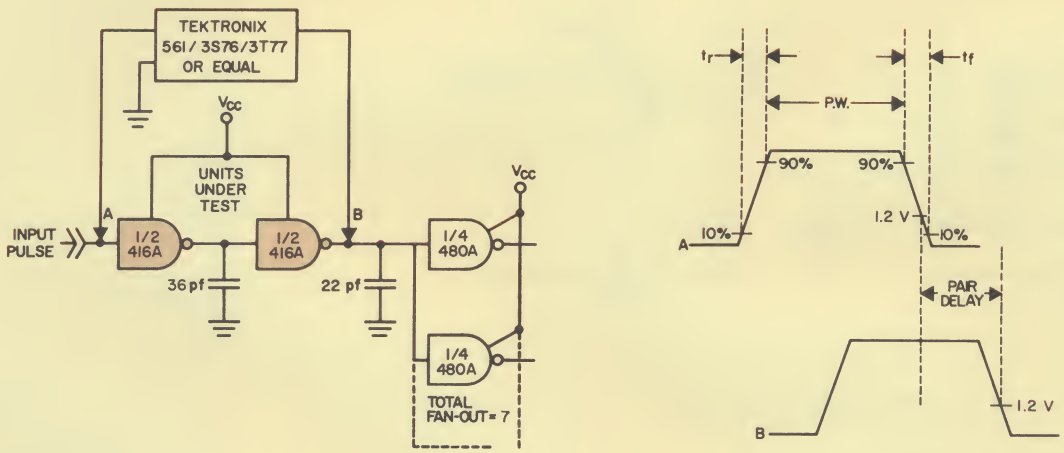
ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4, 5, 6) V_{CC}=5.0V±5%

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNITS	TEMP.	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	3.2			V	0°C	0.8V		-180μA	8
A-3		3.2			V	+25°C	0.8V		-180μA	8
A-4		3.2			V	+70°C	0.8V		-180μA	8
A-5	"0" OUTPUT VOLTAGE			0.35	V	0°C	2.0V	2.0V	7.0 mA	
A-3				0.35	V	+25°C	2.0V	2.0V	7.0 mA	
A-4				0.35	V	+70°C	2.0V	2.0V	7.0 mA	
C-1	"0" INPUT CURRENT			-1.5	mA	0°C	0.35V			
A-3				-1.5	mA	+25°C	0.35V			
C-1				-1.5	mA	+70°C	0.35V			
A-4	"1" INPUT CURRENT			25	μA	+70°C	5.0V	0V		
	PAIR DELAY (Figure 1)		65		ns	+25°C			DC F.O.=7	9
	INPUT CAPACITANCE		3.0		pf	+25°C	2.0V			7
	AVERAGE POWER CONSUMPTION PER GATE		9.0		mW	+25°C				11
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	50μA	0V		
	DC FAN-OUT	7								9, 10

NOTES:

(1) All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
(2) All measurements are taken with Pin 7 tied to zero volts.
(3) Positive current flow is defined as into the terminal referenced.
(4) Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
(5) Precautionary measures should be taken to ensure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.
(6) Measurements apply to each gate element independently.
(7) Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent, f = 1 MHz, Vac = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests.
(8) Output leakage current is supplied through a resistor to ground.
(9) DC fan-out is defined in terms of SIGNETICS Standard Unit Load, which is an NE480A gate input or an equivalent impedance.
(10) This is not a test point, but is guaranteed as a result of calculations using guaranteed test points.
(11) Measured at 50 percent duty cycle.

FIGURE 1 — PAIR DELAY



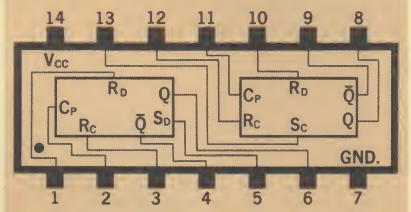
NOTES: (1) Capacitance values shown include probe and test fixture capacitance.
(2) Input Pulse Characteristics: Amplitude=+2.7 V; f=1.0 MHz; PW=350 ns; t_r=t_f≃10 ns.

LOW POWER MONOLITHIC ELEMENT

DUAL AC BINARY

NE424A

OCTOBER 1966



The NE424A is a monolithic silicon integrated circuit containing two RS/T binary elements in a 14-lead dual in-line package. The device is designed to operate in low power digital systems at frequencies up to 10 MHz over the operating temperature range of 0°C to 70°C.

The same planar and epitaxial techniques used in fabricating the SE400J-Series elements are employed in making the NE400A-Series. These elements are tested under the appropriate portion of Signetics established SURE Program (Systematic Uniformity and Reliability Evaluation), as described in Bulletin No. 5001. Acceptance Test Sub-Groups called out in the tabular data refer to selection and test criteria as specified in Table II of SURE Program Bulletin No. 5001.

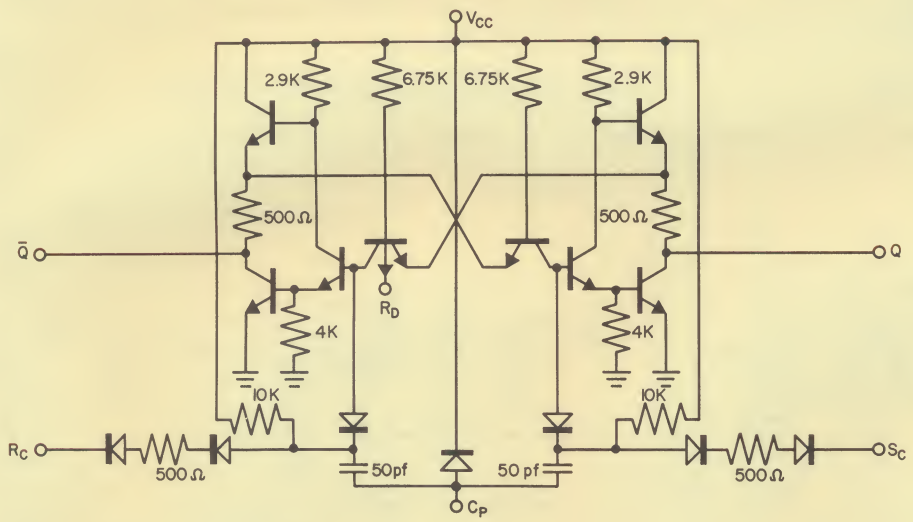
TRUTH TABLE

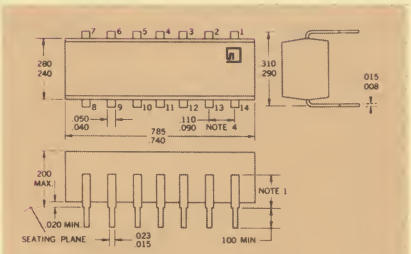
R_C	S_C	Q_{N+1}
1	0	1
0	1	0
1	1	No Change
0	0	?

$R_D=0 \Longrightarrow Q=0$

BASIC CIRCUIT SCHEMATIC

NOTE: ½ of NE424A shown. Component values are typical.





NOTE:
1. Lead spacing shall be measured within this zone.
2. Molded Plastic Body.
3. Kovar Leads.
4. Lead spacing tolerances are non-cumulative.
5. Thermal resistance from junction to still air, Θ_{J-A}= 0.16°C/mW

ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE	6.0V	OPERATING TEMP.	0°C to +70°C
V_{cc}	6.0V	STORAGE TEMP.	-65°C to +150°C
INPUT CURRENT	±10mA	θ JUNCTION TO CASE	0.2°C/mW
OUTPUT CURRENT	+30, -10mA	JUNCTION TEMP.	150°C

Maximum ratings are limiting values above which serviceability may be impaired.

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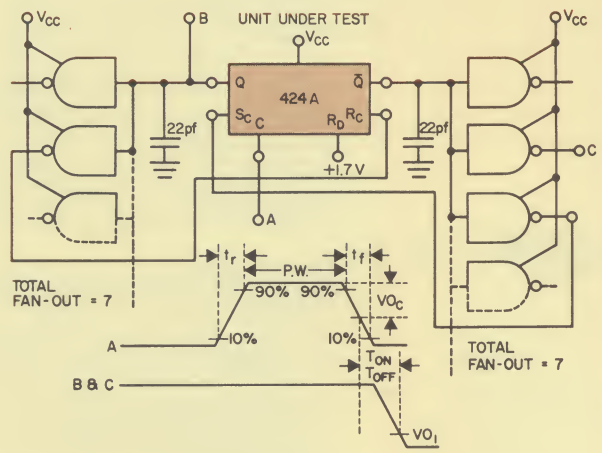
ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4, 5, 6) V_{CC}=5.0V±5%

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP.	R_D	CLOCK	S_C	R_C	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE $Q, \bar{Q}$	3.2			V	0°C	0.8V				-180μA	8, 9
A-3		3.2			V	+25°C	0.8V				-180μA	8, 9
A-4		3.2			V	+70°C	0.8V				-180μA	8, 9
A-5	"0" OUTPUT VOLTAGE $Q, \bar{Q}$			0.35	V	0°C	2.0V				7.0 mA	
A-3				0.35	V	+25°C	2.0V				7.0 mA	
A-4				0.35	V	+70°C	2.0V				7.0 mA	
A-5	"0" INPUT CURRENT R_D			-1.0	mA	0°C	0.35V					
A-3	R_D			-1.0	mA	+25°C	0.35V					
A-4	R_D			-1.0	mA	+70°C	0.35V					
A-5	S_C, R_C			-0.6	mA	0°C			0V	0V		
A-3	S_C, R_C			-0.6	mA	+25°C			0V	0V		
A-4	S_C, R_C			-0.6	mA	+70°C			0V	0V		
A-3	CLOCK			-500	nA	+25°C		0V				
	TURN-ON DELAY (Figure 1)		45		ns	+25°C					F.O.=7	10
	TURN-OFF DELAY (Figure 1)		45		ns	+25°C					F.O.=7	10
	AVERAGE POWER CONSUMPTION PER BINARY		14		mW	+25°C			Q	$\bar{Q}$		12
C-2	TOGGLE SPEED		9.0		MHz	+25°C			Q	$\bar{Q}$		
C-2	OUTPUT FALL TIME (Figure 2)			75	ns	+25°C					AC F.O.=2	11
	INPUT CAPACITANCE											
	CLOCK		50		pf	+25°C		2.0V				7
	R_D		3.0		pf	+25°C	2.0V					7
	S_C, R_C		3.0		pf	+25°C			2.0V	2.0V		7
A-2	INPUT VOLTAGE RATING											
	R_D	6.0			V	+25°C	-50μA					
	CLOCK	5.0			V	+25°C		-10μA	0V	0V		
	DC FAN-OUT	7										10

NOTES

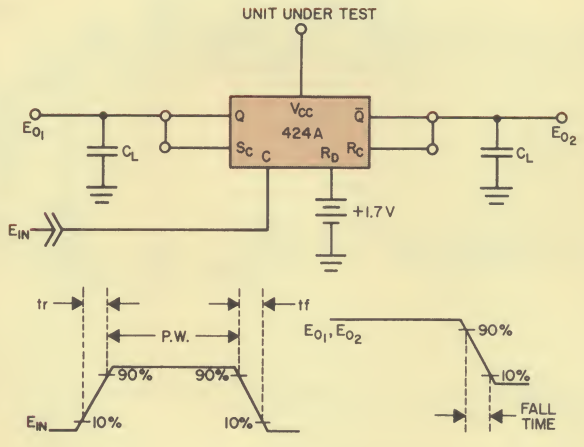
(1) All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
(2) All measurements are taken with Pin 7 tied to zero volts.
(3) Positive current flow is defined as into the terminal referenced.
(4) Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
(5) Precautionary measures should be taken to ensure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.
(6) Measurements apply to each binary element independently.
(7) Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent, f = 1 MHz, Vac = 25mV$_{rms}$. All pins not specifically referenced are tied to guard for capacitance tests.
(8) The binary Q side is set in a "1" by clocking once with the R_C line high and the S_C line low, R_D set at 2.0V. For alternate $\bar{Q}$ test S_C is set high, R_C low and the binary clocked once.
(9) Output leakage current is supplied through a resistor to ground.
(10) DC fan-out is defined in terms of a Signetics Standard Unit Load, which is an NE480A gate input or an equivalent impedance.
(11) One AC fan-out is defined as equivalent to one clock pulse input of an NE424A or a 50 pf capacitance load.
(12) Measured at 50 percent duty cycle.

FIGURE 1—CLOCKED MODE TURN ON AND TURN OFF DELAY



NOTES: (1) Input Pulse Characteristics: Amplitude=+2.7 V; PW=200 ns; f=1 MHz; t_r=t_f≃15 ns.
(2) V_{OC}=1.7 V.
(3) All gates are ¼ 480A

FIGURE 2—OUTPUT FALL TIME CIRCUIT



NOTES: (1) Input Pulse Characteristics: Amplitude=+2.7 V; PW=200 ns; t_r=t_f≃15 ns.
(2) C_L=187 pf, Fan-out=3 at +25°C.
(3) Measurements made with Tektronix Inc. 3S76/3T77/561A.

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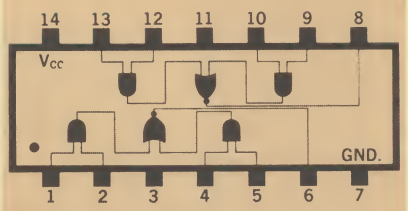
LOW POWER MONOLITHIC DTL ELEMENT

DUAL EXCLUSIVE OR GATE

NE440A

OCTOBER 1966

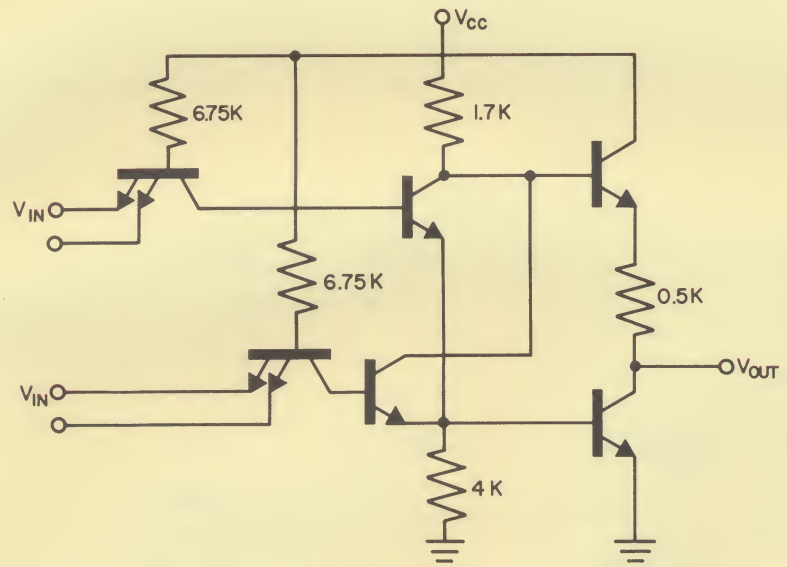


The NE440A is a monolithic semiconductor integrated circuit designed for use in low power digital systems. The element provides for implementation of the Exclusive-OR function in the logic system.

The same planar and epitaxial techniques used in fabricating the SE400J-Series elements are employed in making the NE400A-Series. These elements are tested under the appropriate portion of Signetics established SURE Program (Systematic Uniformity and Reliability Evaluation), as described in Bulletin No. 5001. Acceptance Test Sub-Groups called out in the tabular data refer to selection and test criteria as specified in Table II of SURE Program Bulletin No. 5001.

BASIC CIRCUIT SCHEMATIC

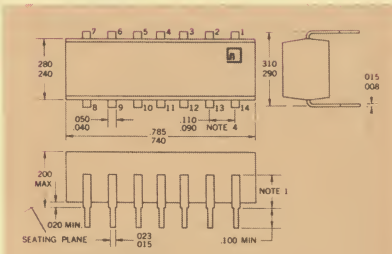
NOTE: ½ of NE440A shown. Component values are typical.



ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE	6.0V	OPERATING TEMP.	0°C to +70°C
V_{cc}	6.0V	STORAGE TEMP.	-65°C to +150°C
INPUT CURRENT	±10mA	θ JUNCTION TO CASE	0.2°C/mW
OUTPUT CURRENT	+30, -10mA	JUNCTION TEMP.	150°C

Maximum ratings are limiting values above which serviceability may be impaired.



NOTE:
1. Lead spacing shall be measured within this zone.
2. Molded Plastic Body.
3. Kovar Leads.
4. Lead spacing tolerances are non-cumulative.
5. Thermal resistance from junction to still air, $\Theta_{J-A} = 0.16°C/mW$

NE440A

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ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4, 5, 6) V_{CC}=5.0V±5%

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNITS	TEMP.	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	3.2			V	0°C	0.8V		-180μA	8
A-3		3.2			V	+25°C	0.8V		-180μA	8
A-4		3.2			V	+70°C	0.8V		-180μA	8
A-5	"0" OUTPUT VOLTAGE			0.35	V	0°C	2.0V	2.0V	7.0 mA	
A-3				0.35	V	+25°C	2.0V	2.0V	7.0 mA	
A-4				0.35	V	+70°C	2.0V	2.0V	7.0 mA	
C-1	"0" INPUT CURRENT			-1.0	mA	0°C	0.35V			
A-3				-1.0	mA	+25°C	0.35V			
C-1				-1.0	mA	+70°C	0.35V			
A-4	"1" INPUT CURRENT			25	μA	+70°C	5.0V	0V		
	PAIR DELAY (Figure 1)		50		ns	+25°C			DC F.O.=7	9
	INPUT CAPACITANCE		3.0		pf	+25°C	2.0V			7
	AVERAGE POWER CONSUMPTION PER GATE		10		mW	+25°C				12
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	50μA	0V		
	DC FAN-OUT	7								9, 11

NOTES

(1) All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specificially referenced are left electrically open.
(2) All measurements are taken with Pin 7 tied to zero volts.
(3) Positive current flow is defined as into the terminal referenced.
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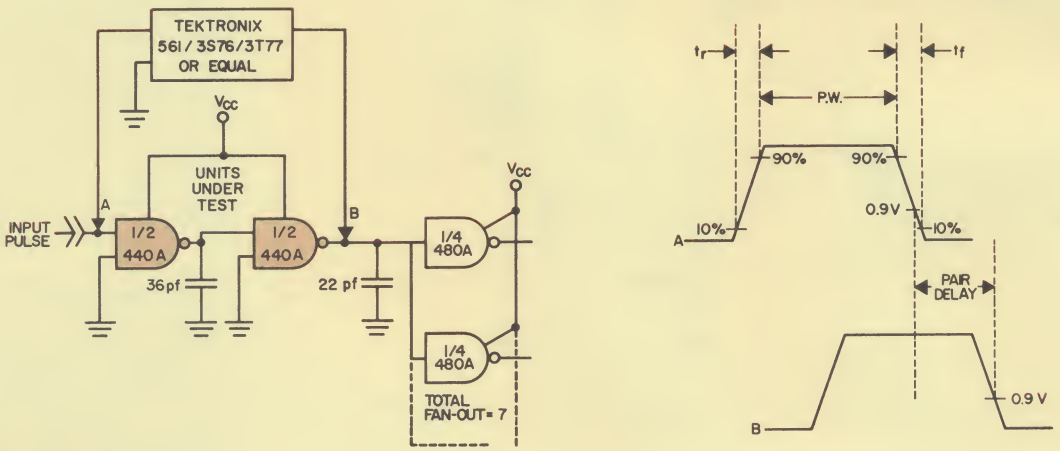
(8) Output leakage current is supplied through a resistor to ground.
(9) DC fan-out is defined in terms of Signetics Standard Unit Load, which is an NE480A gate input or an equivalent impedance.
(10) One AC fan-out is defined as equivalent to one clock pulse input of an NE424A or a 50 pf capacitance load.
(11) This is not a test point, but is guaranteed as a result of calculations using guaranteed test points.
(12) Measured at 50 percent duty cycle.

FIGURE 1 — PAIR DELAY



NOTES: (1) Capacitance values shown include probe and test fixture capacitance.
(2) Input Pulse Characteristics: Amplitude=+2.7 V; f=1.0 MHz; PW=350 ns; t_r=t_f≃10 ns.